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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,836	02/02/2001	Richard Bisinella	CALLINAN 207-KFM	1154

7590 12/16/2003

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/775,836	Applicant(s) BISINELLA, RICHARD	
	Examiner Eric Coleman	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3,5 are rejected under 35 U.S.C. 102(b) as being anticipated by Pechanek (patent No. 5,682,544) in view of Pechanek (patent No. 5,640,586).

3. Pechanek '544 taught the invention as claimed including a data processing ("DP") system comprising:

a) Program control (e.g., see col. 4, lines 38-49 and col. 12, lines 33-35 and fig. 5C);

b) Registers (e.g., see fig.3A, 3B, and col. 3, line 31-col. 8, line 5)

b) Arithmetic logic units (e.g., see fig. 4 and col. 4, lines 37-59 and col. 8, lines 5-67);

d) Input/output circuits (SW1, SW2)(e.g., see fig. 4, and col. 8, lines 5-67).

4. Pechanek '544 did not expressly detail all the elements were on the same chip or comprised a single microprocessor. Pechanek '586 however taught the system with program control, registers, arithmetic logic units, input/output circuits on the same chip (e.g., see col, 22, lines 4-56, figs. 1c, 1d, and col. 20, line 34-col. 21, line 62).

5. Pechanek '544 claimed priority from Pechanek '586 and incorporated the teachings of Pechanek '586 by reference (e.g., see col. 1, lines 62-67 of Pechanek '544).

6. Pechanek '544 taught the components (registers ALU and switches) were selectively connected under program control (e.g.; see col. 6, line 31 -col. 8, line 67).

7. As per claims 2,3, Pechanek '544 taught that that the interconnection was on a grid and connections between components switched under program control (e.g., see col. 4, lines 37-59 and col. 6, line 5-col. 8, line 67).

8. As per claim 5, Pechanek '544 taught connecting that grid to a further grid in a massively parallel system (e.g., see fig. 5C and col. 4 lines 37-49). Pechanek '544 also taught the connection of plural chips for building massive parallel processors was known in the art (e.g., see col. 3, line 13-col. 4, line 28). Pechanek '586 also taught the basic building block chip could be connected to other building block chips to build a scalable system (e.g., see abstract).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek (patent No. 5,682,544) in view of Pechanek (patent No. 5,640,586).

11. Pechanek '544 taught the invention as substantially as claimed including a data processing ("DP") system comprising:

a) Program control (e.g., see col. 4, lines 38-49 and col. 12, lines 33-35 and fig. 5C);

b) Registers (e.g., see fig.3A,3B, and col. 3 line 31-col. 8, line 5)

b) Arithmetic logic units (e.g., see fig. 4 and col. 4, lines 37-59 and col. 8, lines 5-67);

d) Input/output circuits (SW1,SW2)(e.g., see fig. 4, and col. 8, lines 5-67).

12. Pechanek '544 did not expressly detail all the elements were on the same chip or comprised a single microprocessor. Pechanek '586 however taught the system with program control, registers, arithmetic logic units, input/output circuits on the same chip (e.g., see col, 22, lines 4-56, figs. 1c, 1d, and col. 20, line 34-col. 21, line 62).

13. Pechanek '544 claimed priority from Pechanek '586 and incorporated the teachings of Pechanek '586 by reference (e.g., see col. 1, lines 62-67 of Pechanek '544).

14. Pechanek '544 taught the components (registers ALU and switches) were selectively connected under program control (e.g., see col. 6, line 31 -col. 8, line 67).

15. As per claims 2,3, Pechanek '544 taught that that the interconnection was on a grid and connections between components switched under program control (e.g., see col. 4, lines 37-59 and col. 6, line 5-col. 8, line 67).

16. As to the decoder and clock limitation of claim 4, Pechanek '544 taught instruction decoding means in each processing element (e.g., see col. 15, lines 13-17).

Also Pechanek '544 taught SIMD and MIMD mode operation of prior art massively parallel processors (e.g., see col. 3, lines 13-59). These modes required synchronization of the processing elements. Therefore one of ordinary skill in the DP art would have been motivated to providing clocking to the array of processing elements register and I/O components for providing properly timed operation at least when operating in SIMD or MIMD modes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kung (patent No. 4,807,183) disclosed programmable interconnection chip for computer system functional modules (e.g., see abstract).

Mock (patent No. 3,940,744) disclosed a self-contained program loading system (e.g., see abstract and fig. 1).

Wang (patent No. 5,187,796) disclosed a three-dimensional vector coprocessor with plural ALUs selectively connected to vector register file via multiplexers (e.g., 3).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

EC

ERIC COLEMAN
PRIMARY EXAMINER

December 11, 2003